

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 1-3 without prejudice.

1-3 (Cancelled)

1 4. (New) A computer system comprising:  
2 a central processing unit (CPU) having:  
3 a CPU core;  
4 cache memory having a plurality of cache lines, each of the plurality of  
5 cache lines being compressible to form compressed cache lines to store additional  
6 data; and  
7 compression/decompression logic; and  
8 a memory controller coupled to the CPU having a compression map to indicate  
9 whether a cache line corresponding to a block of data in a system memory is in a  
10 compressed format.

1 5. (New) The computer system of claim 4 wherein the compression map includes  
2 bits that provides status for each aligned block in the system memory.

1 6. (New) The computer system of claim 4 wherein the compression/decompression  
2 logic compresses cache line data with a companion cache line as the data is passed from  
3 the CPU core to the cache memory.

1 7. (New) The computer system of claim 4 wherein the compression/decompression  
2 logic compresses cache line data with a companion cache line prior to the data being  
3 passed to the system memory.

1 8. (New) The computer system of claim 4 wherein the compression/decompression  
2 logic compresses cache line data with a companion cache line prior to the data being  
3 passed to a second CPU.

1 9. (New) The computer system of claim 4 wherein CPU further comprises a buffer  
2 to temporarily store cache line data prior to the data being compressed at the  
3 compression/decompression logic.

1 10. (New) The computer system of claim 4 further comprising:  
2 a first interface to communicate with components that transmit and receive  
3 uncompressed cache line data; and  
4 a second interface to communicate with components that transmit and receive  
5 compressed cache line data.

11. (New) The computer system of claim 4 further comprising cache coherency  
logic.

1 12. (New) A method comprising:  
2 compressing one or more of a plurality of cache lines to form one or more  
3 compressed cache lines; and

4 updating a compression map within a memory controller to indicate the one or  
5 more cache lines corresponding to a block of data in a system memory are in a  
6 compressed format.

1 13. (New) The method of claim 12 further comprising storing the compressed cache  
2 lines in a cache memory.

1 14. (New) The method of claim 12 wherein updating the compression map comprises  
2 updating a status bit associated with the block of data.

1 15. (New) The method of claim 12 further comprising buffering data corresponding  
2 to the cache lines prior to compressing the cache lines.

16. (New) The method of claim 13 further comprising transmitting the compressed  
cache lines to the system memory.

1 17. (New) A central processing unit (CPU) comprising:  
2 a CPU core;  
3 a cache memory having a plurality of cache lines, each of the plurality of cache  
4 lines being compressible to form compressed cache lines to store additional data;  
5 compression/decompression logic; and  
6 a memory controller having a compression map to indicate whether a cache line  
7 corresponding to a block of data in a system memory is in a compressed format.

1 18. (New) The CPU of claim 17 wherein the compression map includes bits that  
2 provides status for each aligned block in the system memory.

1 19. (New) The CPU of claim 17 wherein the compression/decompression logic  
2 compresses cache line data with a companion cache line as the data is passed from the  
3 CPU core to the cache memory.

1 20. (New) The CPU of claim 17 wherein the compression/decompression logic  
2 compresses cache line data with a companion cache line prior to the data being passed to  
3 the system memory.

1 21. (New) The CPU of claim 17 wherein the compression/decompression logic  
2 compresses cache line data with a companion cache line prior to the data being passed to  
3 a second CPU.

1 22. (New) The CPU of claim 17 wherein CPU further comprises a buffer to  
2 temporarily store cache line data prior to the data being compressed at the  
3 compression/decompression logic.

1 23. (New) The CPU of claim 17 further comprising:  
2 a first interface to communicate with components that transmit and receive  
3 uncompressed cache line data; and  
4 a second interface to communicate with components that transmit and receive  
5 compressed cache line data.